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Photovoltaic Manufacturing Technology Phase I, Final Report

Final Subcontract Report
9 January 1991 - 14 April 1991

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On September 16, 1991, the Solar Energy Research Institute was designated a national laboratory, and its name was changed to the National Renewable Energy Laboratory.

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SUMMARY

1.1 Objective

The objective of this Phase I contract is to identify:

A) Current capabilities in manufacturing and process development for wafers, solar cells and modules.

B) Manufacturing potentials envisioned to lead to significantly increased production capabilities and reduced manufacturing costs.

C) Problems impeding the achievements of those potentials.

D) Cost and other requirements involved in overcoming the problems in manufacturing technology.

1.2 Scope of Work

The scope of work in this contract includes:

A) Describe the overall procedure that is used by GPS to manufacture wafers, solar cells and modules. This description specifies any technology from other companies or sources upon which the subcontractor is reliant.

B) Identify and describe potential manufacturing processes or changes to existing processes that can lead to improved performance, reduced manfuacturing costs, significantly increased production, and the long range potential benefits of these improved processes.

C) Identify and describe the problems that may impede the achievement of the potential benefits described in (B) above. Identify all generic problems for which GPS is seeking solutions.

D) Identify the approaches which can be taken for the solution of problems identified in C) above including the time- and cost-estimates for achieving those solutions.

1.3 Conclusions

Global Photovoltaic Specialists,Inc. has completed the 4 Tasks as outlined in the Statement of Work and these are delineated in the subsequent sections of this report.

Section 2

CURRENT CAPABILIITY FOR PHOTOVOLTAIC MANUFACTURE

2.1 Background of GPS

Global Photovoltaic Specialists,Inc. is a 10-year old company whose principal activities are in the following areas:

A) low-cost direct silicon wafer formation

B) processes and automation for large-scale manufacture

C) turnkey crystalline silicon factory technology

D) specialized maufacturing equipment for module assembly

GPS is currently expanding its manufacturing capabilities to 5MW using semicrystalline silicon material that is sliced into thin wafers for solar cell and module manufacture. Some of the equipment used in the integrated manufacturing process is purchased from outside suppliers, such as ingot casting furnaces, screen printers, infrared conveyor furnaces for drying, AR coating deposition and thick film sintering.

Other equipment is fabricated by outside suppliers in accordance with GPS specifications, such as wet etching lines, spraying systems, and diffusion furnaces. In a third category, GPS designs and fabricates proprietary equipment for module assembly. This includes:

A) manual and automated solar cell testing

B) mechanized and fully automated solar cell circuit interconnection and formation

C) vacuum transfer and handling of module circuit

D) lamination equipment

E) fully automated meter-mix dispensing equipment for the use of liquid encapsulants of circuits

F) robotic equipment for small shingle circuit assembly

G) large-area pulsed solar simulator for module testing

In addition, GPS is working on strategic relationships with outside suppliers for the automation of wafer handling through conveyor furnaces for a variety of applications. Recently GPS announced that it has commericalized a liquid dopant that can be sprayed onto wafers for large-scale emitter formation.

2.2 Description of Current Manufacturing Processes

2.2.1 Ingot casting and slicing

Figure 2-1 shows the process scheme for the casting and slicing of semicrystalline silicon wafers. The formation of the ingot is done in a modified Bridgman furnace that can produce ingots up to about 100 kilograms(yielded) in a time period of about 41 hours. The resulting ingot is then sectioned both to remove unusable portions and to provide an appropriate brick size that will be used in the slicing operation. Each casting furnace has a capacity of about 1.25 million 10 x 10cm wafers annually.

The sectioned bricks are then corner-ground to provide cropped or rounded corners in order to reduce mechanical damage in later cell processing. The bricks are then sliced on a commercial wire saw that has a capacity of about 7,000-10 x 10cm wafers on a 3-shift basis. On an annual basis this saw can produce over 2 million wafers. In the final step of the wafer preparation they are subjected to an aqueous cleaning process in which the oil-based cutting slurry, silicon carbide abrasive and other debris from the silicon are removed and then rinsed in cascading deionized water. Drying is performed using warm, dry, HEPA filtered air that is a by-product of the waste heat in the ingot casting process.

2.2.1.1 Description of equipment and suppliers

The equipment used in the ingot casting and slicing operations are as follows:

	Process	Equipment	Supplier
A)	ingot casting	Bridgman furnace	Crystalox, England
B)	ingot sectioning	band saw	Everett, U.S.
C)	corner grinding	surface grinder	K.O. Lee, U.S.
D)	wafer slicing	wire saw	HCT, Switzerland
E)	wafer cleaning	cleaning line	various(GPS design)

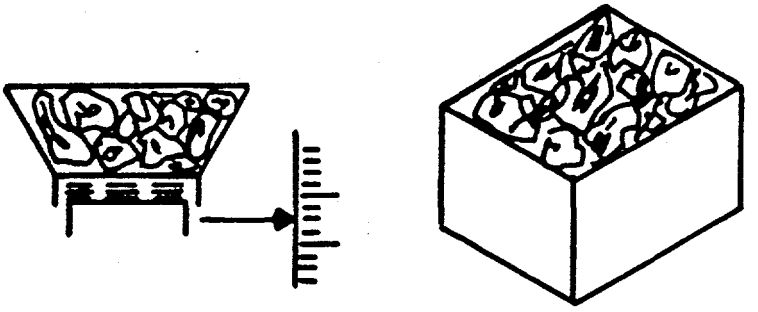
2.2.1.2 Capital costs and estimated finished wafer cost

The approximate cost for this capital equipment excluding leasehold improvements and installation and a production capacity of about 2 million wafers(yielded) annually is $2.75 million. The cost of the finished wafer 10 x 10 x .025cm is $1.03.

FIGURE 2-1

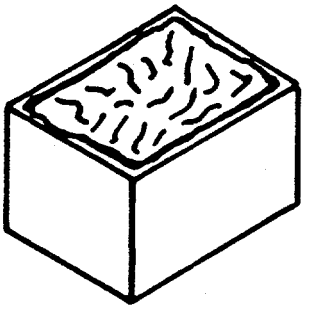
INGOT CASTING & SLICING

WEIGH–DOPE SILICON

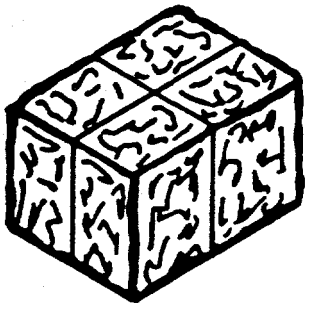


100KG.

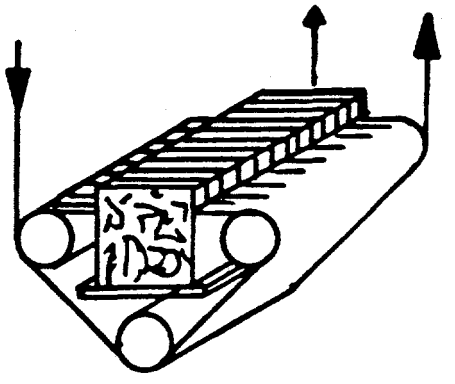
CAST INGOT



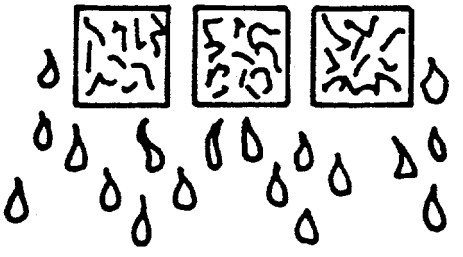
SECTION INGOT



SLICE WAFERS



CLEANWAFERS



2.2.2 Solar cell manufacture

Figure 2-2 exhibits the process scheme for solar cell manufacture currently used.

A) Damage etch

The saw damage etch typically removes a total of 30-40 microns of wire saw-damaged silicon using a hot alkaline solution in a cycle time of about 10 minutes. The wafers are then rinsed in cascading deionized(DI) water.

B) Texturization

While primarily used for single crystal silicon, this anisotropic etch is also used for the 30% crystallites on semicrystalline silicon that have the <100> orientation. A hot, dilute alcohol-alkaline solution requires about 25-30 minutes cycle time. After cascade rinsing in DI water the wafers are neutralized in a dilute acid solution before the final DI water rinse. The wafers are then dried with warm HEPA-filtered air similar to that used after the post-slicing cleaning.

C) Emitter diffusion

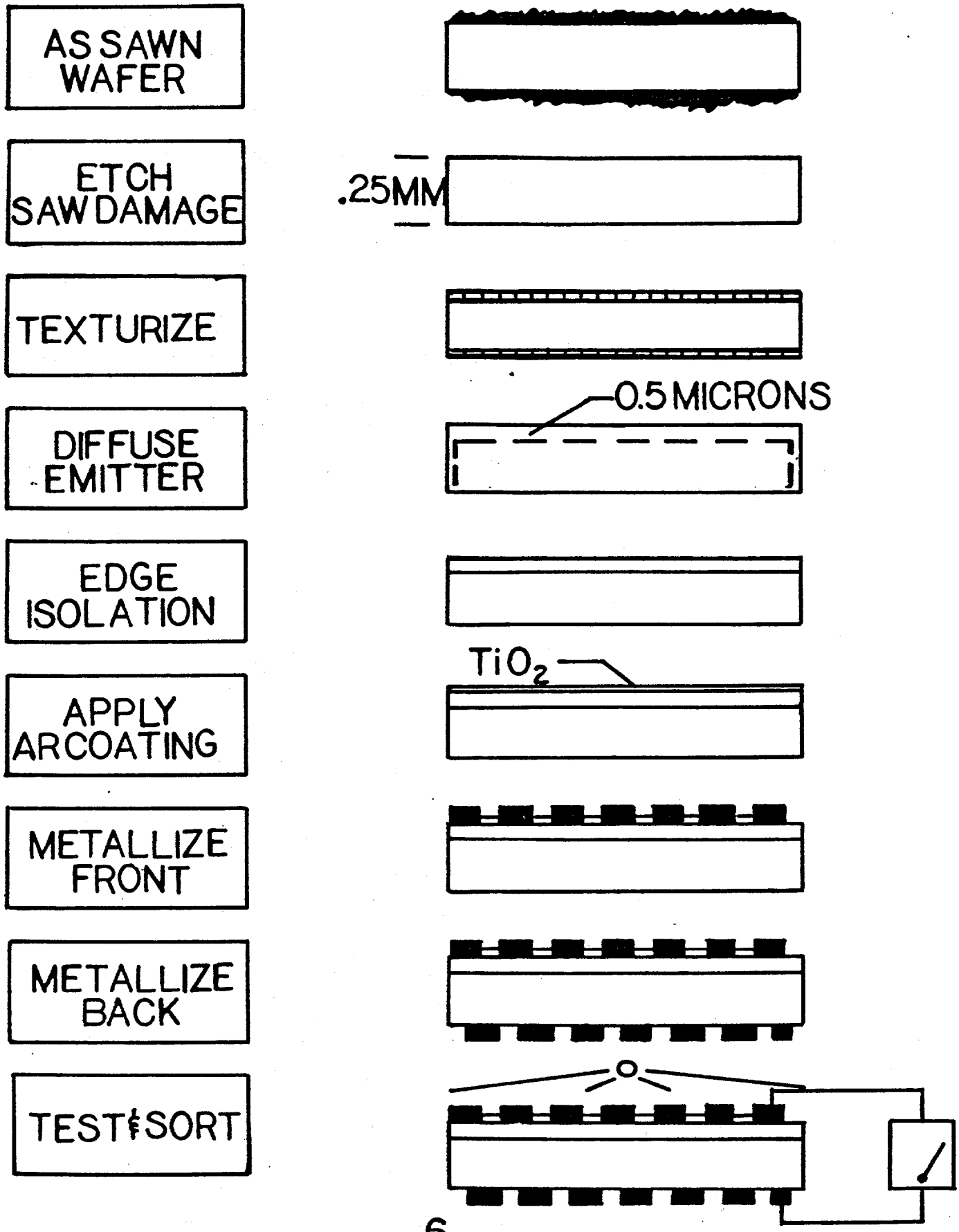
A proprietary liquid dopant is automatically sprayed onto wafers that are close-spaced on a conveyor within a HEPA filtered chamber that provides for laminar flow. These wafers then proceed into an infrared drying furnace section in which the dopant layer is dried of volatile solvent. The wafers are then transfered with the active surfaces facing each other into a high temperature conveyor furnace wherein the emitter is formed in about 20 minutes.

D) Edge separation

The wafers are placed in a coin stack and compressed with appropriate weight in a dry plasma etching chamber in which the dopant layer at the perimeter of the wafer is removed. This batch process has a cycle time of about 30 minutes. The wafers are then loaded into an etching cassette and subjected to dilute acid for diffusion glass removal. DI water rinsing and drying is conducted as in previously described sections.

FIGURE 2-2

SOLAR CELL PROCESS SEQUENCE



E) AR coating deposition

The antireflection coating of titanium dioxide is deposited in a conveyorized atomospheric pressure chemical vapor deposition(APCVD) system. This system uses the organo-titanium precursor of titanium isopropoxide. Upon reaction at the hot surface of the solar cell TiO2 is deposited to coating thickness of about 75 nanometers.

F) Screen printed metallization

In the first of a 2-step operation, one side of the solar cell is printed with the prescribed pattern and subjected to a conveyorized IR drying. The cells then proceed to a second screen printer and the second side of the cell is printed and subjected to a second IR conveyorized dryer and firing furnace in which the thick film silver metallization is sintered.

G) Electrical testing

Under a simulated one-sun condition, solar cells are tested under controlled temperature near the maximum power point and sorted into different current categories.

2.2.2.1 Description of equipment and suppliers

The equipment used in solar cell manufacture are as follows:

	Process	Equipment	Supplier
A)	damage etch	etching line	various(GPS design)
B)	texturization	etching line	various(GPS design)
C)	emitter diffusion	spray system IR dryer/furnace	Zicon(GPS), U.S. BTU International, U.S.
D)	Edge isolation	plasma etcher wet etch	Branson, Tegal, U.S. various(GPS design)
E)	AR coating	APCVD furnace	BTU International, U.S.
F)	Metallization	printer/furnace	AMI, BTU, U.S.
G)	Electrical test	1-sun tester	GPS design/manufacture

2.2.2.2 Capital costs and estimated solar cell cost

The approximate cost for this capital equipment excluding leasehold improvements and installation and a production capacity of about 5 million solar cells(yielded) annually is $2 million. The cost of the finished solar cell is $1.28/Wp.

2.2.3 Module assembly

Figure 2-3 shows the assembly process for module assembly that is currently used.

A) Circuit string interconnection

The interconnection of the circuit string is conducted in a fully automated machine that accepts coin stacks of pre-sorted solar cells. In the first step solder paste is applied to both the front and back of the cell which is then transported to the ribbon application portion of the machine. In this operation dual ribbons of solder plated copper are dispensed to the moving line of cells and the ribbons are sheared to length. As the cells are conveyed further, they are heated with the applied ribbons and solder reflowed to the corresponding front and back areas of the cells. The now-interconnected and continuous series circuit proceeds through a warm ultrasonic solution in which residual solder flux is removed. As the circuit emerges from the flux removal operation, it is cut to length and transported over to the circuit assembly operation.

B) Module circuit formation

In this operation multiple circuit strings are end-connected for continuity as well as terminated using solder ribbon preforms. This is a manually conducted soldering operation.

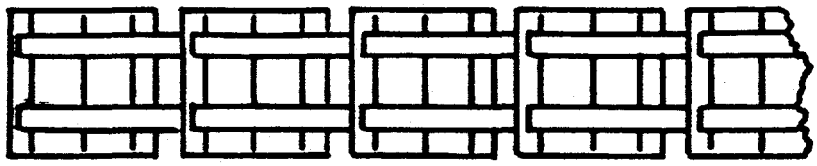
C) Module layup

Figure 2-4 exhibits the module details and construction. The circuit is vacuum-transfered to the layup station at which the various elements of the module packaging are added.

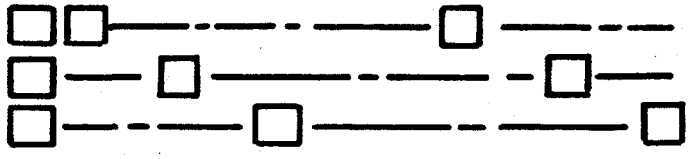
FIGURE 2-3

MODULE ASSEMBLY SEQUENCE

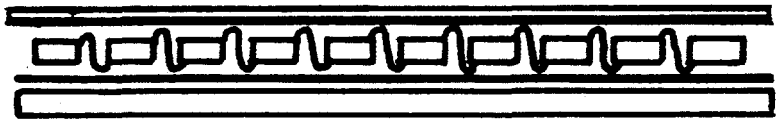
CONNECT STRING



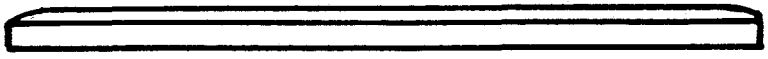
FORM CIRCUIT



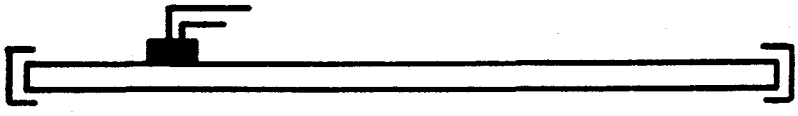
MODULE LAYUP



LAMINATION & CURE



FRAME & TERMINATE



TEST & SHIP

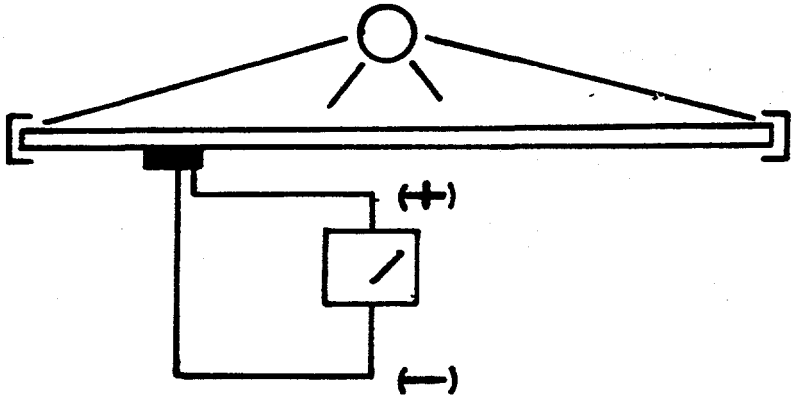
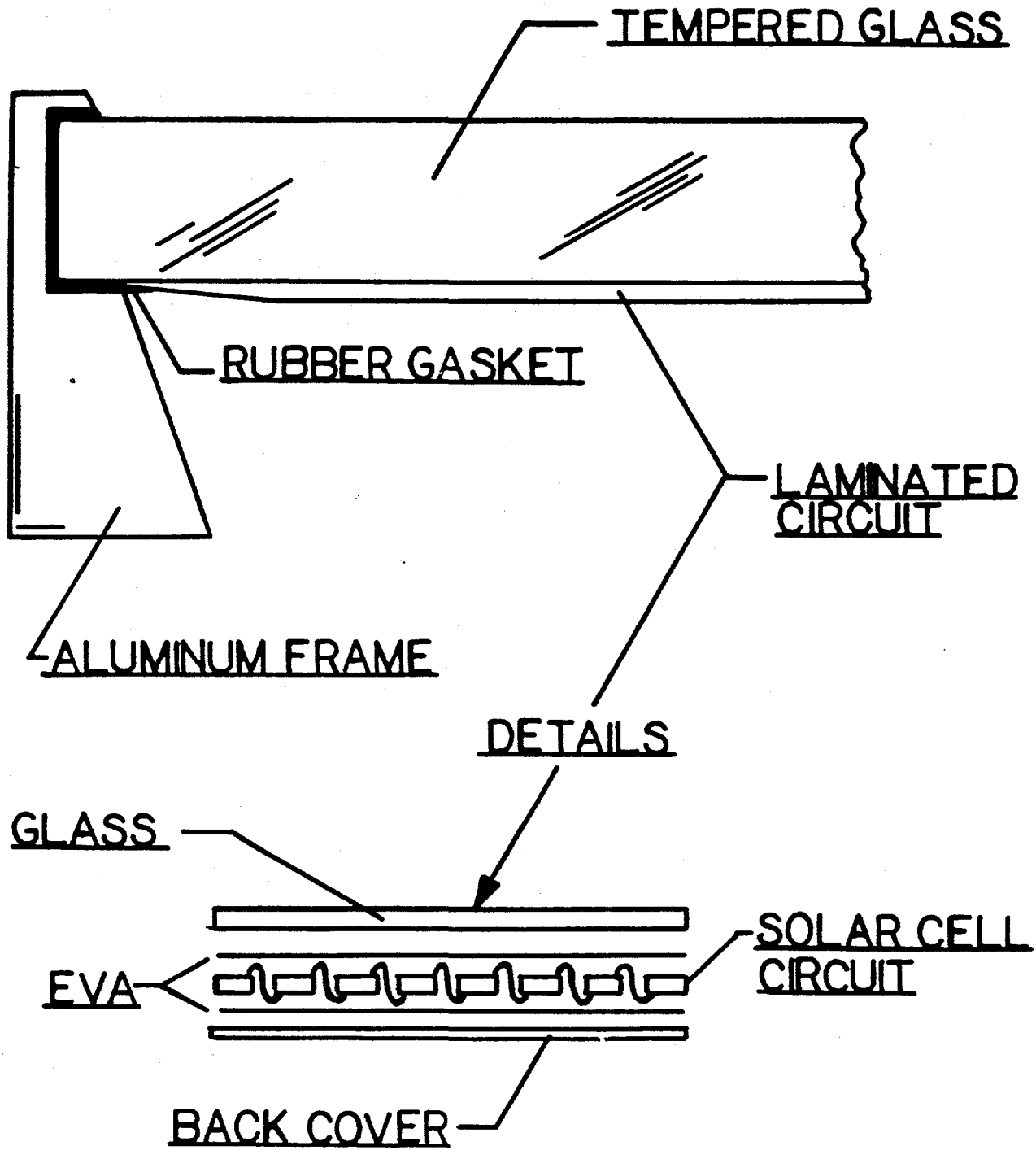


FIGURE 2-4

MODULE ELEMENTS



D) Lamination and in-situ cure

In the lamination step the module layup is placed onto the hot platen of the laminator and after closing it is evacuated of air. After atmospheric backfilling of the flexible bladder, the module is compressed while still under vacuum and the hot melt lamination film is fully cured. This process cycle takes about 8 minutes.

E) Framing and circuit termination

In this final assembly operation, the rubber gasket is applied at glass perimeter and the frame is attached and closed. The junction box or other termination is connected with solder plated copper ribbons that emerge through slits in the back cover of the module(usually a Tedlar*-polyester layer). If a junction box is used, it is both adhesively bonded to the back cover and mechanically attached to the frame at one edge of the module.

F) Electrical test

In this final electrical test, the module is tested under simulated one-sun conditions using a large-area pulsed solar simulator(LAPSS).

2.2.3.1 Description of equipment and suppliers

The equipment used in module assembly is as follows:

	Process	Equipment	Supplier
A)	circuit interconnect	automated	GPS, U.S.
B)	module layup	vacuum transfer	GPS, U.S.
C)	lamination	laminator	GPS, U.S.
D)	electrical test	LAPSS	GPS, U.S.

2.2.3.2 Capital cost and estimated module cost

The approximate cost for this capital equipment excluding leasehold improvments and installation and a production capacity of about 5MW(yielded) annually is $2 million. The cost of the finished module is $2.66/Wp.

* Tedlar is a Dupont trademark

2.3 Source of Technology

Global Photovoltaic Specialists,Inc. does not rely on nor obtain technology in this integrated manufacture from other suppliers. Much of what is currently known about such manufacture is available in the public domain, and proprietary modifications have been applied to improve these processes. While much of the equipment that is used for manufacture is purchased as off-the-shelf, GPS does purchase some of this equipment with proprietary modifications and also manufactures a line of proprietary module assembly equipment.

SECTION 3

MODIFICATIONS AND MANUFACTURING POTENTIALS

3.1 Proposed Changes and New Processes

3.1.1 Crystal growth and wafer formation

GPS has developed a proprietary method for the direct formation of semicrystalline silicon wafers using rapid quenching in a mold(1). This process has the potential to completely eliminate the energy intensive and wasteful crystal growing process and the subsequent slicing.

While the development of this process is being undertaken as proprietary to GPS, the subsequent treatments that are suggested could, in fact, lead to improved wafer charactertistics in terms of resulting solar cell efficiency. For example, it is well known that the gettering of impurities via a number of processes improves the conversion efficiency of solar cells. Similarly, it has been well demonstrated that passivation of the grain boundaries in semicrystalline silicon can lead to improved performance(2,3).

3.1.1.1 Gettering of Direct-Cast wafer

Because the mold-cast wafer is likely to have metallic impurities that must be removed as a part of the wafer preparation, a process that includes some form of high temperature diffusion in which the heavy metal impurties are captured in the resulting glass layer is suggested. This may take the form of the classic chlorine gettering in which volatile metal halides are formed and removed and/or a phosphorous diffusion process in which the grains are passivated while heavy metals are gettered into the glass layer which is subsequently removed.

3.1.1.2 Passivation of the grain boundaries

Because of the electrical activity of grain boundaries in semicrystalline silicon, it is desirable to passivate these grains using phosphorous diffusion. There is also a large body of work that clearly shows the benefits of hydrogen passivation of the surface which can lead to improved cell performance(4,5). With the work that GPS has already conducted into the use of rapid thermal processing for emitter formation, such a technique may be of value in both grain passivation and gettering of the cast wafer in a more rapid and energy-efficient process(6).

3.1.1.3 Wafer surface patterning via mold replication

Because semicrystalline silicon does not lend itself to the conventional anisotropic etching for the reduction of surface reflection except in a limited manner, other means of patterning the surface have been sought(7). GPS's SILCAST wafer process uses a mold to define the finished wafer. In earlier work it has been found that a reduction in the surface roughness of the mold coating can improve the removal characteristics and reduce wafer breakage using very thin wafers(8). One method that may, in fact, provide a reproducible method of wafer surface texture is to pattern the mold itself. Since the mold is used numerous times before the coating must be refurbished, the cast wafer could replicate the mold coating surface texture in-situ and thus eliminate the need for texturizing the wafer in a secondary process.

BENEFITS OF IMPROVMEMENTS IN WAFER FORMATION:

1. Table 3-1 shows the costs and assumptions that have been used for the first production-scale machine to produce Direct-Cast wafers in a mold. This projected wafer cost is about 20% of that of the current grown and sliced wafer or about $.24.

2. While significantly less in cost than conventionally-produced wafers, SILCAST must still be able to consistently produce efficient solar cells with near or comparable conversion efficiencies. The proposed treatments to the mold-cast wafer have the potential to improve the base wafer characteristics to achieve the targeted goal.

3.1.2 Solar cell manufacture

GPS has already commenced activities in the last year with the level of automation and computer integrated manufacture(CIM) that will be necessary for very large-scale solar cell production. This is related to the installation of the world's first 25MW factory using semicrystalline silicon(9,10). The proposed modified manufacturing process sequence is illustrated in Figure 3-1. The major elements of this scheme are CIM and full automation; fully conveyorized processes that are operated using wafer coin stacks are common to all equipment; all wet processes have been converted from batch-type to conveyor; virtually all equipment that is planned for such a CIM factory is available with standard RS232 computer ports, and additional sensors that permit accurate measurement of process parameters have been incorporated. This includes mass flow contollers, optical recognition and other means for ensuring statistical process control and the resulting high process yields.

TABLE 3-1

*
SILCAST WAFER COSTS

COST MODEL ASSUMPTIONS

* ASSUME $4 MILLION FOR MACHINE WITH CAPACITY OF 10MW

* POLYSILICON COSTS OF $18/KILOGRAM

* ASSUME 95% YIELD IN THE CASTING OF THE WAFER

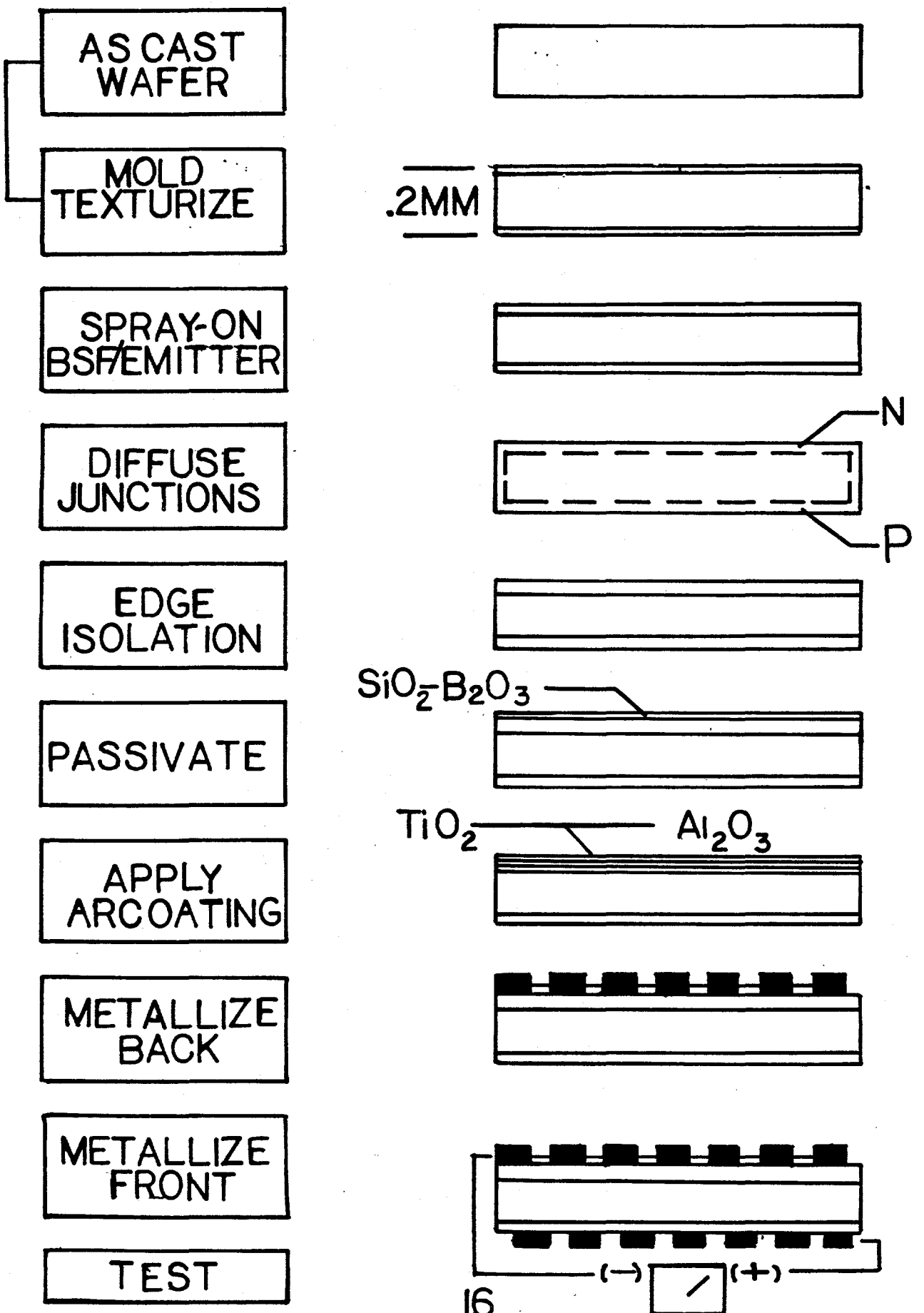
* WAFER THICKNESS IS 200 MICRONS THICK, 10 X 10CM

1.	SILICON COST(4.9 GRAMS)	$.09
2.	EQUIPMENT AMORTIZATION(7 YEARS)	.06
3.	LABOR(6/SHIFT X 3 SHIFTS)	.03
4.	RENT/ELECTRICITY	.02
5.	MISCELLANEOUS	.01
6.	OVERHEAD	.03
	TOTAL WAFER COST	$.24

* SILCAST is a trademark of Global Photovoltaic Specialists,Inc.

FIGURE 3-1

SOLAR CELL PROCESS SEQUENCE



3.1.2.1 Wafer etching(eliminated)

Because the mold-cast wafer does not have slicing damage and is expected to obtain surface texture by replication in the mold, the classic alkaline etching for saw damage removal and texturization can be eliminated. While this process is only a small part of the cost of solar cell manufacture, it does represent an additional 16% loss of silicon even with the use of wire sawn wafers(this assumes 250 micron thick wafer and 40 microns of silicon etched).

3.1.2.2 Emitter/back surface field formation with RTP

Rapid thermal processing using spray-on dopants has already demonstrated the potential for efficient solar cells both for the emitter and emitter-back surface field(11,12). GPS has also developed and is currently commericalizing a liquid dopant for N-type emitter formation. With thin wafers a BSF is expected to improve conversion efficiency, and the simultaneous formation of the emitter and BSF using RTP is in keeping with the reqirements of very large-scale production. Diffusion glass removal will also be changed from a batch-type operation to an enclosed and conveyorized etching, deionized water rinse, and warm air drying process. This etching operation will be loaded and unloaded from wafer coin stacks identical to other conveyorized processes described.

3.1.2.3 Edge isolation

This process will remain the same as before using a series of wafer coin stacks that are already an established mechanism for the automated handling of wafers in the production line. While still a batch operation, the coin stacks can be processed as received, and the equipment throughput will enable a balanced production line.

3.1.2.4 Surface passivation

In addition of hydrogen passivation, a thin layer of oxide has been shown to reduce surface recombination velocity and hence improve the solar cell's conversion efficiency(13,14). GPS proposes to use a thin, spray-on, low-melting borosilicate glass as a passivation coating. The advantage of this approach is that it can both passivate the surface and permit the direct sintering of the printed thick film metallization without the need for using photolithographic patterning of the coating.

3.1.2.5 Antireflection coating(AR)

This process remains the same and will be used in conjunction with a passivation coating through which the thick film metallization can be sintered to the silicon. A dual ARC with the addition of Al2O3 is suggested to the current scheme.

3.1.2.6 Ink jet printing of metallization

While the scheme for solar cell metallization remains the same, the method of ink jet printing for the thick film paste has the potential for reducing the shadowing effect by printing lines in the order of 50-75 microns in width as compared to the 125-150 microns of conventional screen printing. The other side benefit is that less thick film ink will be used in the process. While preliminary work has shown the potential for this process, both the equipment and thick film ink formulations require considerable investigation before they can demonstrate the applicability of this process to very large-scale solar cell manufacture. Additionally, while the current metallization is sintered to the silicon through the current AR coating of TiO2, additional investigation of this fire-through process will have to be conducted in conjunction with the use of the proposed spray-on passivation coating.

3.1.2.7 Electrical testing

This step in the cell manufacturing process remains unchanged.

BENEFITS OF THE PROPOSED CHANGES IN CELL PROCESSES:

1. The major benefits in the proposed cell process sequence are improved throughput, reduced operating costs with fewer energy intensive operations, reduced material requirements, enhanced solar cell conversion efficiency, and lower overall solar cell cost/peak watt produced.

2. Another consideration in solar cell manufacture is the increase in solar cell size from 10 x 10cm to 15 x 15cm because of what is perceived as needed for large-area modules for the emerging utility and home-electric markets. Since the proposed module size is of the order of 1.2 x 2.4m and that utility application will likely have uniform module current and voltage requirements, increased cell size will reduce production handling throughput while increasing production capacity by 125%.

3.1.3 Module assembly

3.1.3.1 Circuit interconnection and assembly

The only change to the current sequence for automated module interconnection is to combine the circuit formation step with the series string interconnection.

3.1.3.2 Module layup

This step in the sequence remains unchanged.

3.1.3.3 Lamination

The increased size of the proposed module for utility and home-electric markets requires that the module size increase in area to as much as 8 times that currently used. Because of the manufacturing scale and module size, a radical approach is taken to module lamination. While the process is identical to that currently used with the so-called double vacuum and flexible diaphragm, the equipment for lamination would be designed so that a series of laminator plates be vertically combined in a hydraulic press that would be automatically loaded and unloaded with these large-area modules. In the lamination process, the press would close the plates into a single system with evacuation, compression with the bladder, and in-situ cure. Figure 3-2 illustrates what form this might take.

3.1.3.4 Framing and circuit termination

This step in the sequence remains unchanged.

3.1.3.5 Electrical test

This step in the sequence remains unchanged.

BENFITS OF PROPOSED CHANGES TO MODULE ASSEMBLY:

1. Since most of the module assembly has already been automated, the changes in the initial assembly of the circuit combine the interconection and assembly into a single machine.

2. Because of the significantly increased size of the module for utility and home electric markets, a new approach to module lamination can reduce handling and the risk of module breakage. This approach also provides the automated factory with increased throughput while reducing labor content.

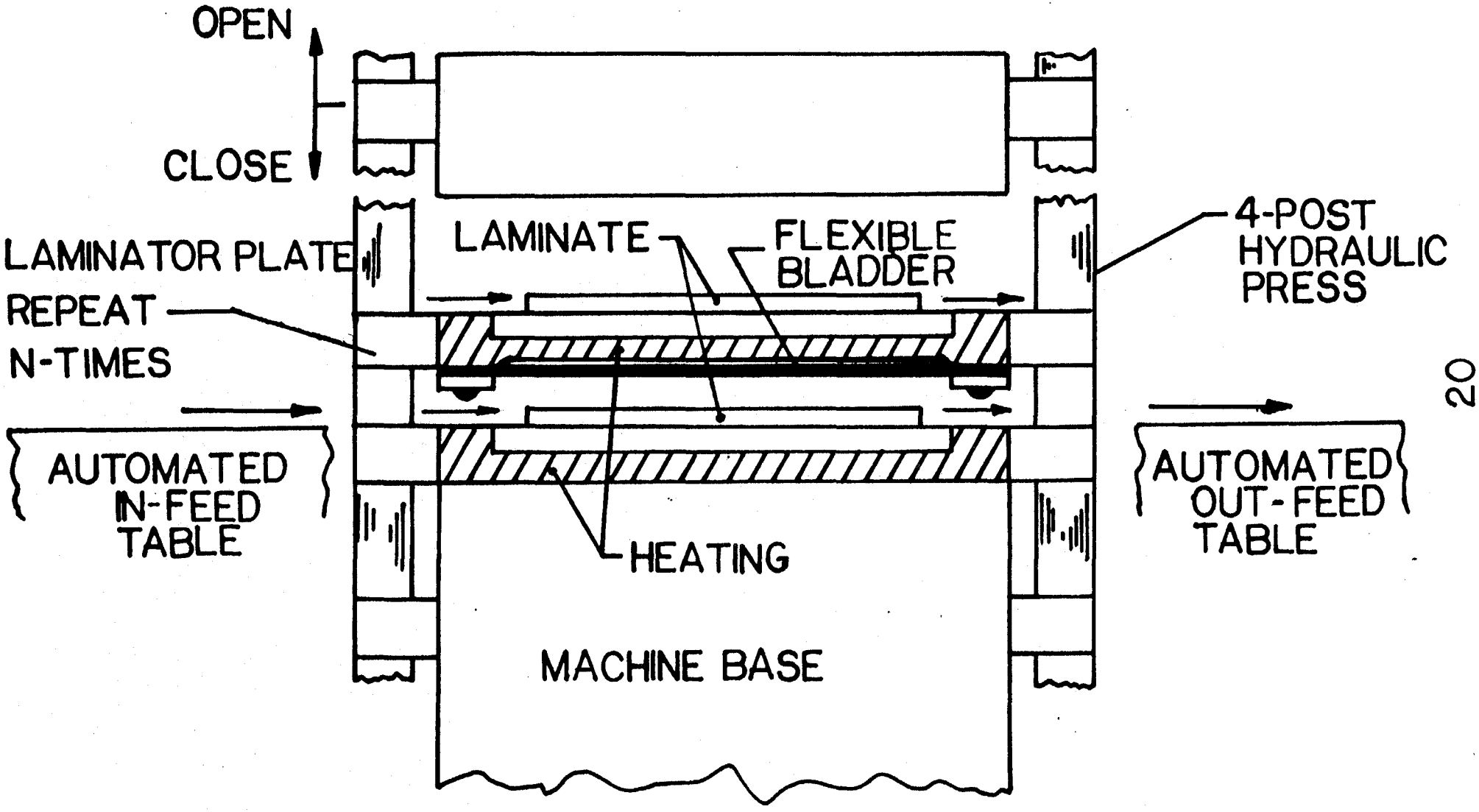
3.2 Long Range Benefits of the Proposed Changes

3.2.1 Low-cost cast wafer

The major benefit of the proposed changes is to introduce a low-cost material with improved characteristics that can lead to significant reductions in wafer cost, currently the highest cost element in photovoltaic manufacture and major impediment to a finished module with a selling cost of less than $2.00/Wp.

FIGURE 3-2

VERTICALLY STACKED LAMINATION



3.2.2 Automation and improved cell characteristics

The recommended changes to the solar cell process sequence can result in significantly improved conversion efficiencies. It is estimated that with a BSF, surface passivation, dual ARC, and reduced metallization shadowing, there could be a gain of as much as 1.5% in absolute efficiency. Automation and the elimination of batch-type processes will reduce labor content in manufacture, and with CIM the factory can provide improved throughput with higher material yields.

3.2.3 Changes in module assembly

While only limited changes are proposed in the assembly of the module, increased module sizes require an improvement in the handling of the module layup into and out of the lamination process. The vertically stacked lamination approach can result in substantially reduced handling and subseqent module breakage, and it will also provide greater throughput in the assembly of the module.

SECTION 4

PROBLEMS AND IMPEDIMENTS IN ACHIEVING PRESCRIBED SOLUTIONS

4.1 Silicon Wafer Formation

4.1.1 In-situ wafer texture

In previous work it was shown that a reduction of the mold coating surface roughness improved the removability of thin wafers from the mold with reduced breakage(8). Because of the requirements of wafer surface texture to achieve reduced surface reflection, there may have to be a compromise in the roughness of the mold coating and surface texturization in order to obtain both ease of removal and an acceptable level of texture on the wafer surface. Currently it is possible to control the surface roughness of the mold coating through the parameters of refractory deposition. The coating can be currently patterned by laser ablation and shot peening. Other than preliminary work in the deposition of this coating, it is not known if the deposition process or other processes can themselves be tailored to provide the desired surface finish and texture.

4.1.2 Wafer gettering and passivation

The conventional methods for gettering have been associated with high temperature and long process cycles in order to remove impurities; this is counterproductive to the rapid wafer formation process. This is similarly the case for grain boundry passivation using phorphorous diffusion methods. Rapid thermal processing may offer a compromise to achieve these goals while using the subsequent spray-on emitter/BSF process to anneal out damage such as vacancies, interstitials, etc.

4.2 Solar Cell Processes

4.2.1 RTP for emitter/BSF formation

While RTP has already been demonstrated to have some utility for emitter formation, combining the emitter and BSF in the same process considering the difference in the diffusion coefficients of phosphorous and boron may require a change in the base material used. While it has been proposed that quenched-in defects from wafer gettering and passivation be annealed out in this solar cell process step, it is not known what problems, if any, will be encountered after emitter/BSF formation. At least a portion of this problem is considered generic as the spray-on diffusion process is becoming generic with commercialization of liquid dopants for solar cell emitter formation.

4.2.2 Ink jet printing

This process holds substantial promise for reducing gridline shadowing on the front of the solar cell and also reduces the amount of material used. Additionally, this approach to solar cell metallization is more benign for very thin silicon wafers. The principal difficulties that are anticipated are the definition and development of equipment suitable for large-scale manufacture and the development that will be necessary in concert with any selected thick film ink supplier. As is the case with conventional screen printing, ink jet printing is considered a generic problem since the development and commericalization of the equipment and thick film ink can only be accomplished if it conducted in the public domain.

4.3 Module Assembly

4.3.1 Lamination

GPS has already commenced work on the design and fabrication of the prototype of the described vertical lamination system. As GPS expects to commericalize this lamination system along with the automated loading and unloading systems for large-area modules, this is considered to be a generic problem in the industry as the need for large-area modules for utility and home electric markets emerge in high volume production.

SECTION 5

PROPOSED SOLUTIONS AND TIME-COST ESTIMATES

5.1 Silicon Wafer Preparation

5.1.2 Mold surface modification for in-situ wafer texture

GPS proposes that a range of deposition methods and parameters be investigated for the refractory coating on the mold. These include flame spray, plasma-arc spray and electric-arc spray chemical vapor depostion, sputtering and ion plating.

The important features of the deposited coating in the order of priority are:

1. durability for re-use for numerous wafer castings.

2. surface roughness and ease of wafer removal from the mold.

3. surface texture for replication in the wafer in order to reduce light reflection.

5.1.2.1 Time an cost estimates for resolution

1. 4 man-years for conducting deposition experiments, laser ablation, shot peening, and wafer casting. Approximately $300,000.

2. Outside services for having the mold coated by a variety of techniques and depostion parameters, laser ablation and shot peening of the coating. Approximately $200,000.

3. Other administrative costs of $50,000.

5.1.3 Wafer gettering and passivation

A variety of gettering and passivation processes will be attempted using in-house equipment and personnel. These will include coventional chlorine gettering, phosphorous diffusion and rapid thermal processing, wafer backside damaging and gettering, BSF aluminum, hydrogen passivation and using such coatings as borosilicate passivation in conjunction with these techniques.

5.1.3.1 Time and cost estimates for resolution

1. 4 man-years for conducting the experiments using a variety of gettering and passivation methods. Approximately $300,000.

2. Material and outside analytical services for this work. $150,000.

3. Other administrative costs of $45,000.

5.2 Solar Cell Processes

5.2.1 Simultaneous emitter/BSF formation using RTP

This efforts will focus on the application of spray-on liquid dopants for the emitter and BSF and conveyorized RTP and annealing of damage. This anealing will also be examined for improving the characteristics of the wafer gettering/passivation using RTP. These experiments will also examine the addition of printed dopants for locally diffused regions below the areas of metallization so that an optimized emitter/metallization structure may be obtained.

5.2.1.1 Time and cost estimates for resolution

1. 6 man-years for conducting the spray-on development, experiments in diffusion, equipment design for conveyorized RTP, and localized dopant printing for locally diffused emitter formation. Approximately $450,000.

2. Materials and outside analytical services for this work. $125,000.

3. Other administrative costs of $57,500.

5.2.2 Ink jet printing of metallization

1. 3 man-years for conducting the in-house experiments and the assistance in the design of the equipment with an outside supplier. $225,000.

2. Thick film ink material and outside analytical services. $100,000.

3. Other administrative costs of $32,500.

5.3 Module Assembly

5.3.1 Design and fabrication of vertical lamination

This work will require the design and protypical fabarication of the lamination system proposed along with the automated handling of large-area modules.

5.3.1.1 Time and cost estimate for resolution

1. 2 man-years for the design and prototypical testing of the proposed laminator design and automated module handling apparatus. $150,000

2. Materials and outside drafting services and fabrication. $75,000.

3. Other administrative costs of $22,500.

5.4 Summary of Estimates for Resolution of Stated Problems

The total time and cost estimate is based upon a 2-year effort. No estimates have been included for capital equipment for this work. Some of the equipment that would be necessary is shown as being contracted with outside experiments being directed by GPS personnel. The total estimated cost for this work is $2,395,000.

SECTION 6

CONCLUSIONS

In this short 3-month study, GPS has examined existing integrated processes for solar cell manufacture and believes that the primary opportunity for improvement can be obtained in the following areas:

1. Low-cost cast silicon sheet with improved characteristics.

2. Large-scale and automated solar cells processes have already been demonstrated, and there is opportunity for improved processes that can lead to cell efficiencies in the range of 14%(encapsulated) for direct-cast wafers.

3. While module assembly has already been automated to a great degree, large-area modules for the emerging utility market require improved handling and lamination.

It is believed that the proposed solutions can lead to finished module costs in the order of $1.55/square meter or a selling price of less than $2.00/Watt.

The problems that may be considered generic to the industry and that have been addressed in this work are as follows:

1. Gettering and passivation of silicon wafers.

2. Spray-on diffusion sources and combined emitter/BSF formation using rapid thermal processing.

3. Spray-on passivation layers.

4. Dual AR coating.

5. Ink jet printing of metallization.

6. Automated handling of large-area modules and associated vertical lamination.

SECTION 7

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This report describes existing integrated processes for solar cell manufacturing and lists as the primary opportunity for improvement the following areas: low-cost silicon sheets with improved characteristics; improved large-scale and automated solar cell processes that can lead to cell efficiencies in the range of 14% (encapsulated) for direct-cast wafers; improved handling and lamination of large-area modules for the emerging utility market. The proposed solutions can lead to finished module costs on the order of $1.55 per square meter or a selling price of less than $2.00/Watt. The problems that may be considered generic to the industry and that have been addressed in this work are as follows: gettering and passivation of silicon wafers; spray-on diffusion sources and combined emitter/back surface field formation using rapid thermal processing; spray-on passivation layers; dual antireflection coatings; ink-jet printing of metallizations; and automated handling of large-area modules and associated vertical lamination.

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